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09/847,487	05/02/2001	Alex S.Y. Koh	SC11499TS	6254

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FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER
THANGAVELU, KANDASAMY

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>23 November 2004</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-27</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-27</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>2 May 2001</u> is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   This communication is in response to the Applicants' Amendment dated

November 23, 2004. Claims 18-27 were amended. Claims 1-27 of the application are

pending. This office action is made non-final.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

3.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

4.   Claims 1-3, 7-10, 12, 13, 18 and 19 are rejected under 35 U.S.C. 103(a) as being

unpatentable over **Araki et al.** (U.S. Patent Application 2001/0007972) in view of **Gruodis et al.**

(U.S. Patent 6,092,225).

4.1   **Araki et al.** teaches Method and apparatus for verifying adequacy of test patterns.

Specifically, as per claim 1, **Araki et al.** teaches a method for capturing simulation output (Page

1, Para 0003); comprising:

        providing a stimulus to a test bench (Page 1, Para 0003);

        providing a device model corresponding to an integrated circuit to the test bench (Page 1,

Para 0006 and 0003); and

        in response to applying the stimulus to the device model through the test bench,

generating a captured simulation (Page 1, Para 0003); the captured simulation comprising

information related to at least one of strobe timing information (Page 3, Para 0022), mixed signal

information (Page 1, Para 0005), and internal memory content information (Page 1, Para 0005).

        Araki et al. does not expressly teach the captured simulation comprising information

related to one of opcode information. **Gruodis et al.** teaches the captured simulation comprising

information related to one of opcode information (CL3, L63 to CL4, L4; CL4, L26-62), because

the opcodes indicate to the vector pattern generator the vectors to be supplied to the tester

channel for each test cycle (CL4, L26-29); and allow the vector pattern generator to perform

vector address repeats and jumps and access one or more vector sequences (CL4, L65 to CL6,

L2). It would have been obvious to one of ordinary skill in the art at the time of Applicants'

invention to modify the method of **Araki et al.** with the method of **Gruodis et al.** that included

the captured simulation comprising information related to one of opcode information. The artisan

would have been motivated because the opcodes would indicate to the vector pattern generator

the vectors to be supplied to the tester channel for each test cycle; and would allow the vector

pattern generator to perform vector address repeats and jumps and access one or more vector

sequences.

Per claim 2: **Araki et al.** teaches that the captured simulation comprises sufficient

information for automatically generating a complete test pattern within a test program

corresponding to the integrated circuit (Page 1, Para 0005).

Per claim 3: **Araki et al.** teaches that the captured simulation captures all communication

through the test bench between the stimulus and the device model (Page 1, Para 0003 and Para

0006).

Per claim 7: **Araki et al.** teaches that the stimulus comprises verification patterns,

drivers, and monitors (Page 1, Para 0003, Para 0005 and Para 0006).

In addition, **Lin et al.** (U.S. Patent 6.651,225) also teaches that the stimulus comprises

verification patterns, drivers, and monitors (CL22, L15-16; CL22, L57-59).

Per claim 8: **Araki et al.** teaches that the stimulus further comprises a simulation

environment corresponding to the device model (Page 1, Para 0006).

Per claim 9: **Araki et al.** teaches that in response to applying the stimulus to the device

model through the test bench, the test bench generates a plurality of simulation parameters

corresponding to the stimulus and device model (Page 1, Para 0003, Para 0005; Page 3, Para

0022); and

the captured simulation is based at least in part on the simulation parameters (Page 1,

Para 0003, Para 0005; Page 3, Para 0022).

4.2   As per Claim 10, **Araki et al.** and **Gruodis et al.** teach the method of claim 1. **Araki et**

al. teaches that the captured simulation comprises information relating to another one of strobe

timing information (Page 3, Para 0022), mixed signal information (Page 1, Para 0005), and

internal memory content information (Page 1, Para 0005).

Araki et al. does not expressly teach that the captured simulation comprises information

relating to another one of opcode information. **Gruodis et al.** teaches that the captured

simulation comprises information relating to another one of opcode information (CL3, L63 to

CL4, L4; CL4, L26-62), because the opcodes indicate to the vector pattern generator the vectors

to be supplied to the tester channel for each test cycle (CL4, L26-29); and allow the vector

pattern generator to perform vector address repeats and jumps and access one or more vector

sequences (CL4, L65 to CL6, L2). It would have been obvious to one of ordinary skill in the art

at the time of Applicants' invention to modify the method of **Araki et al.** with the method of

Gruodis et al. that included the captured simulation comprising information relating to another

one of opcode information. The artisan would have been motivated because the opcodes would

indicate to the vector pattern generator the vectors to be supplied to the tester channel for each test cycle; and would allow the vector pattern generator to perform vector address repeats and jumps and access one or more vector sequences.

4.3   As per claim 12, **Araki et al.** teaches a method for preparing a captured simulation for post-processing (Page 1, Para 0003 and Para 0005; Page 1, Para 0011); comprising:

receiving the captured simulation (Page 1, Para 0003); wherein the captured simulation comprises at least one of strobe timing information (Page 3, Para 0022), mixed signal information (Page 1, Para 0005), and internal memory content information (Page 1, Para 0005);

the captured simulation generated in response to stimulus applied to a device model through a test bench (Page 1, Para 0003);

generating data patterns (Fig. 5, Item 31, 33 and 34; Page 1, Para 0011; Page 2, Para 12 and 13), based at least in part on the one of strobe timing information (Page 3, Para 0022), mixed signal information (Page 1, Para 0005), and internal memory content information (Page 1, Para 0005);

the data patterns capable of being retargettable for a plurality of post-processing tools (Fig. 5, Item 31, 33, 34 and 10); and

providing a first formatted pattern file to a first post-processing tool, the first formatted pattern file based on the data patterns (Fig. 5, Item 31).

Araki et al. does not expressly teach that the captured simulation comprises at least one of opcode information; and generating data patterns based at least in part on the one of opcode information. **Gruodis et al.** teaches that the captured simulation comprises at least one of

opcode information; and generating data patterns based at least in part on the one of opcode

information (CL3, L63 to CL4, L4; CL4, L26-62), because the opcodes indicate to the vector

pattern generator the vectors to be supplied to the tester channel for each test cycle (CL4, L26-

29); and allow the vector pattern generator to perform vector address repeats and jumps and

access one or more vector sequences (CL4, L65 to CL6, L2). It would have been obvious to one

of ordinary skill in the art at the time of Applicants' invention to modify the method of **Araki et**

al. with the method of **Gruodis et al.** that included the captured simulation comprising at least

one of opcode information; and generating data patterns based at least in part on the one of

opcode information. The artisan would have been motivated because the opcodes would indicate

to the vector pattern generator the vectors to be supplied to the tester channel for each test cycle;

and would allow the vector pattern generator to perform vector address repeats and jumps and

access one or more vector sequences.

4.4   As per Claim 13, **Araki et al.** and **Gruodis et al.** teach the method of claim 12. **Araki et**

al. teaches that the captured simulation comprises another one of strobe timing information (Page

3, Para 0022), mixed signal information (Page 1, Para 0005), and internal memory content

information (Page 1, Para 0005); and

        generating the data patterns (Fig. 5, Item 31, 33 and 34; Page 1, Para 0011; Page 2, Para

12 and 13), is further based at least in part on the another one of strobe timing information (Page

3, Para 0022), mixed signal information (Page 1, Para 0005), and internal memory content

information (Page 1, Para 0005).

Araki et al. does not expressly teach that the captured simulation comprises another one

of opcode information; and generating data patterns is further based at least in part on the another

one of opcode information. Gruodis et al. teaches that that the captured simulation comprises

another one of opcode information; and generating data patterns is further based at least in part

on the another one of opcode information (CL3, L63 to CL4, L4; CL4, L26-62), because the

opcodes indicate to the vector pattern generator the vectors to be supplied to the tester channel

for each test cycle (CL4, L26-29); and allow the vector pattern generator to perform vector

address repeats and jumps and access one or more vector sequences (CL4, L65 to CL6, L2). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

modify the method of Araki et al. with the method of Gruodis et al. that included the captured

simulation comprising another one of opcode information; and generating data patterns further

based at least in part on the another one of opcode information. The artisan would have been

motivated because the opcodes would indicate to the vector pattern generator the vectors to be

supplied to the tester channel for each test cycle; and would allow the vector pattern generator to

perform vector address repeats and jumps and access one or more vector sequences.

4.5   As per claim 18, Araki et al. teaches a data pattern generator stored via a computer

readable medium (Fig. 5, Items 32 and 33); comprising:

a first plurality of instructions for receiving the captured simulation (Page 1, Para 0003);

wherein the captured simulation comprises at least one of strobe timing information (Page 3,

Para 0022), mixed signal information (Page 1, Para 0005), and internal memory content

information (Page 1, Para 0005);

the captured simulation generated in response to stimulus applied to a device model

through a test bench (Page 1, Para 0003);

a second plurality of instructions for generating data patterns (Fig. 5, Item 31, 33 and 34;

Page 1, Para 0011; Page 2, Para 12 and 13), based at least in part on the one of strobe timing

information (Page 3, Para 0022), mixed signal information (Page 1, Para 0005), and internal

memory content information (Page 1, Para 0005);

the data patterns capable of being retargettable for a plurality of post-processing tools

(Fig. 5, Item 31, 33, 34 and 10); and

a third plurality of instructions for providing a first formatted pattern file to a first post-

processing tool, the first formatted pattern file based on the data patterns (Fig. 5, Item 31).

Araki et al. does not expressly teach that the captured simulation comprises at least one

of opcode information; and generating data patterns based at least in part on the one of opcode

information. **Gruodis et al.** teaches that the captured simulation comprises at least one of

opcode information; and generating data patterns based at least in part on the one of opcode

information (CL3, L63 to CL4, L4; CL4, L26-62), because the opcodes indicate to the vector

pattern generator the vectors to be supplied to the tester channel for each test cycle (CL4, L26-

29); and allow the vector pattern generator to perform vector address repeats and jumps and

access one or more vector sequences (CL4, L65 to CL6, L2). It would have been obvious to one

of ordinary skill in the art at the time of Applicants' invention to modify the method of **Araki et**

al. with the method of **Gruodis et al.** that included the captured simulation comprising at least

one of opcode information; and generating data patterns based at least in part on the one of

opcode information. The artisan would have been motivated because the opcodes would indicate

to the vector pattern generator the vectors to be supplied to the tester channel for each test cycle;

and would allow the vector pattern generator to perform vector address repeats and jumps and

access one or more vector sequences.

4.6   As per Claim 19, **Araki et al.** and **Gruodis et al.** teach the data pattern generator of claim

18. **Araki et al.** teaches that the captured simulation comprises another one of strobe timing

information (Page 3, Para 0022), and mixed signal information (Page 1, Para 0005); and

generating the data patterns (Fig. 5, Item 31, 33 and 34; Page 1, Para 0011; Page 2, Para

12 and 13), is further based at least in part on the another one of strobe timing information (Page

3, Para 0022), and mixed signal information (Page 1, Para 0005).

Araki et al. does not expressly teach that the captured simulation comprises another one

of opcode information; and generating data patterns is further based at least in part on the another

one of opcode information. **Gruodis et al.** teaches that that the captured simulation comprises

another one of opcode information; and generating data patterns is further based at least in part

on the another one of opcode information (CL3, L63 to CL4, L4; CL4, L26-62), because the

opcodes indicate to the vector pattern generator the vectors to be supplied to the tester channel

for each test cycle (CL4, L26-29); and allow the vector pattern generator to perform vector

address repeats and jumps and access one or more vector sequences (CL4, L65 to CL6, L2). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

modify the data pattern generator of **Araki et al.** with the data pattern generator of **Gruodis et**

al. that included the captured simulation comprising another one of opcode information; and

generating data patterns further based at least in part on the another one of opcode information.

The artisan would have been motivated because the opcodes would indicate to the vector pattern

generator the vectors to be supplied to the tester channel for each test cycle; and would allow the

vector pattern generator to perform vector address repeats and jumps and access one or more

vector sequences.

5.   Claims 4-6 and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Araki et al. (U.S. Patent Application 2001/0007972) in view of **Gruodis et al.** (U.S. Patent

6,092,225), and further in view of **Reise et al.** (U.S. Patent 6,678,625).

5.1   As per Claim 4, **Araki et al.** and **Gruodis et al.** teach the method of claim 1. **Araki et**

al. does not expressly teach that the stimulus and the test bench communicate in accordance with

a predetermined protocol which provides a standard interface between the stimulus and the test

bench. **Reise et al.** teaches that the stimulus and the test bench communicate in accordance with

a predetermined protocol which provides a standard interface between the stimulus and the test

bench (Fig. 4 and Fig. 8; CL6, L49-57; CL7, L53-63; CL8, L24-29), because that allows the test

bench to communicate with the stimulus and the DUT through a channel using standard interface

such as PCI or SCSI, so the operation of the DUT may be tested and verified (CL7, L53-63;

CL8, L24-29). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the method of **Araki et al.** with the method of **Reise et al.** that

included the stimulus and the test bench communicating in accordance with a predetermined

protocol which provided a standard interface between the stimulus and the test bench. The

artisan would have been motivated because that would allow the test bench to communicate with

the stimulus and the DUT through a channel using standard interface such as PCI or SCSI, so the

operation of the DUT may be tested and verified.

5.2   As per Claim 5, **Araki et al.** and **Gruodis et al.** teach the method of claim 1. **Araki et**

al. does not expressly teach that the device model and the test bench communicate in accordance

with a predetermined protocol which provides a standard interface between the device model and

the test bench. **Reise et al.** teaches that the device model and the test bench communicate in

accordance with a predetermined protocol which provides a standard interface between the

device model and the test bench (Fig. 4 and Fig. 8; CL6, L49-57; CL7, L53-63; CL8, L24-29),

because that allows the test bench to communicate with the stimulus and the DUT through a

channel using standard interface such as PCI or SCSI, so the operation of the DUT may be tested

and verified (CL7, L53-63; CL8, L24-29). It would have been obvious to one of ordinary skill in

the art at the time of Applicants' invention to modify the method of **Araki et al.** with the method

of **Reise et al.** that included the device model and the test bench communicating in accordance

with a predetermined protocol which provided a standard interface between the device model

and the test bench. The artisan would have been motivated because that would allow the test

bench to communicate with the stimulus and the DUT through a channel using standard interface

such as PCI or SCSI, so the operation of the DUT may be tested and verified.

5.3   As per Claim 6, **Araki et al.**, **Gruodis et al.** and **Reise et al.** teach the method of claim 5.

Araki et al. does not expressly teach that communication with the device model occurs through

the standard interface between the device model and the test bench. **Reise et al.** teaches that

communication with the device model occurs through the standard interface between the device

model and the test bench (Fig. 4 and Fig. 8; CL6, L49-57; CL7, L53-63; CL8, L24-29), because

that allows the test bench to communicate with the stimulus and the DUT through a channel

using standard interface such as PCI or SCSI, so the operation of the DUT may be tested and

verified (CL7, L53-63; CL8, L24-29). It would have been obvious to one of ordinary skill in the

art at the time of Applicants' invention to modify the method of **Araki et al.** with the method of

Reise et al. that included communication with the device model occurring through the standard

interface between the device model and the test bench. The artisan would have been motivated

because that would allow the test bench to communicate with the stimulus and the DUT through

a channel using standard interface such as PCI or SCSI, so the operation of the DUT may be

tested and verified.

5.4 As per claim 22, **Araki et al.** teaches standard test bench stored via a computer readable

medium (Page 1, Para 0003; Fig. 5); comprising:

a first plurality of instructions for receiving a stimulus (Page 1, Para 0003);

a second plurality of instructions for receiving a device model corresponding to an

integrated circuit (Page 1, Para 0003 and Para 0006);

a third plurality of instructions for generating simulation parameters in response to

applying the stimulus to the device model (Page 1, Para 0003 and Para 0005; Page 3, Para 0022);

a fourth plurality of instructions for creating a captured simulation based at least in part

on the simulation parameters (Page 1, Para 0003 and Para 0005; Page 3, Para 0022);

the captured simulation comprising information related to at least one of strobe timing

information (Page 3, Para 0022), mixed signal information (Page 1, Para 0005), and internal

memory content information (Page 1, Para 0005).

Araki et al. does not expressly teach that standard test bench stored via a computer

readable medium is reusable. **Reise et al.** teaches that standard test bench stored via a computer

readable medium is reusable (Abstract, L11-13; CL1, L60-63; CL1, L32-35), because a

standardized, parameterized and reusable test bench may be readily configured for multiple

device models in a design verification test environment (CL1, L32-35). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

standard test bench of **Araki et al.** with the standard test bench of **Reise et al.** that included the

standard test bench stored via a computer readable medium being reusable. The artisan would

have been motivated because a standardized, parameterized and reusable test bench might be

readily configured for multiple device models in a design verification test environment.

Araki et al. does not expressly teach the captured simulation comprising information

related to at least one of opcode information. **Gruodis et al.** teaches the captured simulation

comprising information related to at least one of opcode information (CL3, L63 to CL4, L4;

CL4, L26-62), because the opcodes indicate to the vector pattern generator the vectors to be

supplied to the tester channel for each test cycle (CL4, L26-29); and allow the vector pattern

generator to perform vector address repeats and jumps and access one or more vector sequences

(CL4, L65 to CL6, L2). It would have been obvious to one of ordinary skill in the art at the time

of Applicants' invention to modify the standard test bench of **Araki et al.** with the standard test

bench of **Gruodis et al.** that included the captured simulation comprising information related to

at least one of opcode information. The artisan would have been motivated because the opcodes

would indicate to the vector pattern generator the vectors to be supplied to the tester channel for

each test cycle; and would allow the vector pattern generator to perform vector address repeats

and jumps and access one or more vector sequences.

Per claim 23: **Araki et al.** teaches that the captured simulation comprises sufficient

information for automatically generating a complete test within a test program corresponding to

the integrated circuit (Page 1, Para 0005).

5.5   As per Claims 24 and 25, **Araki et al., Gruodis et al.** and **Reise et al.** teach the standard

test bench of claim 22. **Araki et al.** teaches that the captured simulation captures all

communication between the stimulus and the device model through the standard test bench; and

all communication with the device model occurs through the standard test bench (Page 1, Para

0003 and Para 0006).

Araki et al. does not expressly teach that standard test bench is reusable. **Reise et al.**

teaches that standard test bench is reusable (Abstract, L11-13; CL1, L60-63; CL1, L32-35),

because a standardized, parameterized and reusable test bench may be readily configured for

multiple device models in a design verification test environment (CL1, L32-35). It would have

been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

standard test bench of **Araki et al.** with the standard test bench of **Reise et al.** that included the

standard test bench being reusable. The artisan would have been motivated because a

standardized, parameterized and reusable test bench might be readily configured for multiple

device models in a design verification test environment.

5.6   As per Claim 26, **Araki et al., Gruodis et al.** and **Reise et al.** teach the standard test

bench of claim 22. **Araki et al.** teaches that the captured simulation comprises information

relating to another one of strobe timing information (Page 3, Para 0022), mixed signal

information (Page 1, Para 0005), and internal memory content information (Page 1, Para 0005).

Araki et al. does not expressly teach that the captured simulation comprises information

related to another one of opcode information. **Gruodis et al.** teaches that the captured

simulation comprises information related to another one of opcode information (CL3, L63 to

CL4, L4; CL4, L26-62), because the opcodes indicate to the vector pattern generator the vectors

to be supplied to the tester channel for each test cycle (CL4, L26-29); and allow the vector

pattern generator to perform vector address repeats and jumps and access one or more vector

sequences (CL4, L65 to CL6, L2). It would have been obvious to one of ordinary skill in the art

at the time of Applicants' invention to modify the standard test bench of **Araki et al.** with the

standard test bench of **Gruodis et al.** that included the captured simulation comprising

information related to another one of opcode information. The artisan would have been

motivated because the opcodes would indicate to the vector pattern generator the vectors to be

supplied to the tester channel for each test cycle; and would allow the vector pattern generator to

perform vector address repeats and jumps and access one or more vector sequences.

6.   Claims 11, 14 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Araki et al. (U.S. Patent Application 2001/0007972) in view of **Gruodis et al.** (U.S. Patent

6,092,225), and further in view of **Lesmeister et al.** (U.S. Patent 6,295,623) and **Fusco** (U.S.

Patent 6,308,292).

6.1   As per Claim 11, **Araki et al.** and **Gruodis et al.** teach the method of claim 1. **Araki et**

al. does not expressly teach that the captured simulation further comprises information relating to

at least one of directionality information. **Lesmeister et al.** teaches that the captured simulation

further comprises information relating to at least one of directionality information (CL6, L37-

46), because the direction information is used to identify the signal as the input signal or the

response signal (output signal) (CL6, L37-40; CL7, L54 to CL8, L2). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

method of **Araki et al.** with the method of **Lesmeister et al.** that included the captured

simulation further comprising information relating to at least one of directionality information.

The artisan would have been motivated because the direction information would be used to

identify the signal as the input signal or the response signal (output signal).

        Araki et al. does not expressly teach that the captured simulation further comprises

information relating to at least one of pin data information. **Lesmeister et al.** teaches that the

captured simulation further comprises information relating to at least one of pin data information

(CL4, L20-24), because the pin data relates each pin of the real integrated circuit to an IC input

or output signal of the device model and indicates how the IC pin is connected to the tester

(CL4, L20-24). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the method of **Araki et al.** with the method of **Lesmeister et al.**
that included the captured simulation further comprising information relating to at least one of
pin data information. The artisan would have been motivated because the pin data would relate
each pin of the real integrated circuit to an IC input or output signal of the device model and
indicate how the IC pin would be connected to the tester.

Araki et al. does not expressly teach that the captured simulation further comprises
information relating to at least one of masking information. **Fusco** teaches that the captured
simulation further comprises information relating to at least one of masking information (Fig. 3;
Abstract, L2-5; CL4, L20-25; CL5, L8-15), because masking information would allow the
expected output in a test pattern to be coded such that the tester does not compare the output
signal with the expected data and always passes the masked output signal during the masked
cycle (CL4, L20-25). It would have been obvious to one of ordinary skill in the art at the time of
Applicants' invention to modify the method of **Araki et al.** with the method of **Fusco** that
included the captured simulation further comprising information relating to at least one of
masking information. The artisan would have been motivated because masking information
would allow the expected output in a test pattern to be coded such that the tester would not
compare the output signal with the expected data and would always pass the masked output
signal during the masked cycle.

Araki et al. does not expressly teach that the captured simulation further comprises
information relating to at least one of partial cyclized information. **Lesmeister et al.** teaches that
the captured simulation further comprises information relating to at least one of partial cyclized
information (CL7, L54 to CL8, L6), because the cyclized information restricts the state changes

in each simulated input signal and in sampling each simulated IC output signal to one particular

time during each system clock signal cycle (CL7, L65 to CL8, L2). It would have been obvious

to one of ordinary skill in the art at the time of Applicants' invention to modify the method of

Araki et al. with the method of **Lesmeister et al.** that included the captured simulation further

comprising information relating to at least one of partial cyclized information. The artisan would

have been motivated because the cyclized information would restrict the state changes in each

simulated input signal and in sampling each simulated IC output signal to one particular time

during each system clock signal cycle.

6.2   As per Claim 14, **Araki et al.** and **Gruodis et al.** teach the method of claim 12. **Araki et**

al. does not expressly teach that the captured simulation further comprises information relating to

at least one of directionality information. **Lesmeister et al.** teaches that the captured simulation

further comprises information relating to at least one of directionality information (CL6, L37-

46), because the direction information is used to identify the signal as the input signal or the

response signal (output signal) (CL6, L37-40; CL7, L54 to CL8, L2). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

method of **Araki et al.** with the method of **Lesmeister et al.** that included the captured

simulation further comprising information relating to at least one of directionality information.

The artisan would have been motivated because the direction information would be used to

identify the signal as the input signal or the response signal (output signal).

     Araki et al. does not expressly teach that the captured simulation further comprises

information relating to at least one of pin data information. **Lesmeister et al.** teaches that the

captured simulation further comprises information relating to at least one of pin data information

(CL4, L20-24), because the pin data relates each pin of the real integrated circuit to an IC input

or output signal of the device model and indicates how the IC pin is connected to the tester

(CL4, L20-24). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the method of **Araki et al.** with the method of **Lesmeister et al.**

that included the captured simulation further comprising information relating to at least one of

pin data information. The artisan would have been motivated because the pin data would relate

each pin of the real integrated circuit to an IC input or output signal of the device model and

indicate how the IC pin would be connected to the tester.

Araki et al. does not expressly teach that the captured simulation further comprises

information relating to at least one of masking information. **Fusco** teaches that the captured

simulation further comprises information relating to at least one of masking information (Fig. 3;

Abstract, L2-5; CL4, L20-25; CL5, L8-15), because masking information would allow the

expected output in a test pattern to be coded such that the tester does not compare the output

signal with the expected data and always passes the masked output signal during the masked

cycle (CL4, L20-25). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the method of **Araki et al.** with the method of **Fusco** that

included the captured simulation further comprising information relating to at least one of

masking information. The artisan would have been motivated because masking information

would allow the expected output in a test pattern to be coded such that the tester would not

compare the output signal with the expected data and would always pass the masked output

signal during the masked cycle.

Araki et al. does not expressly teach that the captured simulation further comprises

information relating to at least one of partial cyclized information. Lesmeister et al. teaches that

the captured simulation further comprises information relating to at least one of partial cyclized

information (CL7, L54 to CL8, L6), because the cyclized information restricts the state changes

in each simulated input signal and in sampling each simulated IC output signal to one particular

time during each system clock signal cycle (CL7, L65 to CL8, L2). It would have been obvious

to one of ordinary skill in the art at the time of Applicants' invention to modify the method of

Araki et al. with the method of Lesmeister et al. that included the captured simulation further

comprising information relating to at least one of partial cyclized information. The artisan would

have been motivated because the cyclized information would restrict the state changes in each

simulated input signal and in sampling each simulated IC output signal to one particular time

during each system clock signal cycle.

6.3   As per Claim 27, Araki et al. and Gruodis et al. teach the standard test bench of claim

22. Araki et al. does not expressly teach that the captured simulation further comprises

information relating to at least one of directionality information. Lesmeister et al. teaches that

the captured simulation further comprises information relating to at least one of directionality

information (CL6, L37-46), because the direction information is used to identify the signal as the

input signal or the response signal (output signal) (CL6, L37-40; CL7, L54 to CL8, L2). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to

modify the standard test bench of Araki et al. with the standard test bench of Lesmeister et al.

that included the captured simulation further comprising information relating to at least one of

directionality information. The artisan would have been motivated because the direction

information would be used to identify the signal as the input signal or the response signal (output

signal).

Araki et al. does not expressly teach that the captured simulation further comprises

information relating to at least one of pin data information. **Lesmeister et al.** teaches that the

captured simulation further comprises information relating to at least one of pin data information

(CL4, L20-24), because the pin data relates each pin of the real integrated circuit to an IC input

or output signal of the device model and indicates how the IC pin is connected to the tester

(CL4, L20-24). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the standard test bench of **Araki et al.** with the standard test

bench of **Lesmeister et al.** that included the captured simulation further comprising information

relating to at least one of pin data information. The artisan would have been motivated because

the pin data would relate each pin of the real integrated circuit to an IC input or output signal of

the device model and indicate how the IC pin would be connected to the tester.

Araki et al. does not expressly teach that the captured simulation further comprises

information relating to at least one of masking information. **Fusco** teaches that the captured

simulation further comprises information relating to at least one of masking information (Fig. 3;

Abstract, L2-5; CL4, L20-25; CL5, L8-15), because masking information would allow the

expected output in a test pattern to be coded such that the tester does not compare the output

signal with the expected data and always passes the masked output signal during the masked

cycle (CL4, L20-25). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the standard test bench of **Araki et al.** with the standard test

bench of **Fusco** that included the captured simulation further comprising information relating to

at least one of masking information. The artisan would have been motivated because masking

information would allow the expected output in a test pattern to be coded such that the tester

would not compare the output signal with the expected data and would always pass the masked

output signal during the masked cycle.

Araki et al. does not expressly teach that the captured simulation further comprises

information relating to at least one of partial cyclized information. **Lesmeister et al.** teaches that

the captured simulation further comprises information relating to at least one of partial cyclized

information (CL7, L54 to CL8, L6), because the cyclized information restricts the state changes

in each simulated input signal and in sampling each simulated IC output signal to one particular

time during each system clock signal cycle (CL7, L65 to CL8, L2). It would have been obvious

to one of ordinary skill in the art at the time of Applicants' invention to modify the standard test

bench of **Araki et al.** with the standard test bench of **Lesmeister et al.** that included the captured

simulation further comprising information relating to at least one of partial cyclized information.

The artisan would have been motivated because the cyclized information would restrict the state

changes in each simulated input signal and in sampling each simulated IC output signal to one

particular time during each system clock signal cycle.

7.   Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Araki et al.** (U.S.

Patent Application 2001/0007972) in view of **Gruodis et al.** (U.S. Patent 6,092,225), and further

in view of **Lesmeister et al.** (U.S. Patent 6,295,623).

7.1   As per Claim 15, **Araki et al.** and **Gruodis et al.** teach the method of claim 12. **Araki et al.** does not expressly teach that the data patterns include cyclized patterns. **Lesmeister et al.** teaches that the data patterns include cyclized patterns (CL7, L54 to CL8, L6), because the cyclized information restricts the state changes in each simulated input signal and in sampling each simulated IC output signal to one particular time during each system clock signal cycle (CL7, L65 to CL8, L2). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Araki et al.** with the method of **Lesmeister et al.** that included the data patterns including cyclized patterns. The artisan would have been motivated because the cyclized information would restrict the state changes in each simulated input signal and in sampling each simulated IC output signal to one particular time during each system clock signal cycle.

8.   Claims 16, 17, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Araki et al.** (U.S. Patent Application 2001/0007972) in view of **Gruodis et al.** (U.S. Patent 6,092,225), and further in view of **Fusco** (U.S. Patent 6,308,292).

8.1   As per Claim 16, **Araki et al.** and **Gruodis et al.** teach the method of claim 12. **Araki et al.** teaches that the first post-processing tool is one of a fault simulator (Page 1, Para 0001. L9-10), and virtual tester (Fig. 5, Item 10; Page 2, Para 0013; Page 2-3, Para 0022).

        Araki et al. does not expressly teach that the first post-processing tool is one of an automatic test equipment (ATE) tester. **Fusco** teaches that the first post-processing tool is one of an automatic test equipment (ATE) tester (CL1, L61-65; CL2, L24-39), because the post

processing tool analyzes the simulation results and generates the test files including test patterns

containing IC input patterns and output patterns used by the automatic test equipment (CL2,

L24-29). It would have been obvious to one of ordinary skill in the art at the time of Applicants'

invention to modify the method of **Araki et al.** with the method of **Fusco** that included the first

post-processing tool being one of an automatic test equipment (ATE) tester. The artisan would

have been motivated because the post processing tool would analyze the simulation results and

generate the test files including test patterns containing IC input patterns and output patterns used

by the automatic test equipment.

8.2   As per Claim 17, **Araki et al., Gruodis et al.** and **Fusco** each the method of claim 16.

Araki et al. teaches providing a second formatted pattern file to a second post-processing tool,

the second formatted pattern file based on the data patterns (Fig. 5, Item 21); and

        the second post-processing tool is another one of a fault simulator (Page 1, Para 0001.

L9-10), and virtual tester (Fig. 5, Item 10; Page 2, Para 0013; Page 2-3, Para 0022).

        Araki et al. does not expressly teach that the second post-processing tool is another one

of an automatic test equipment (ATE) tester. **Fusco** teaches that the second post-processing tool

is another one of an automatic test equipment (ATE) tester (CL1, L61-65; CL2, L24-39),

because the post processing tool analyzes the simulation results and generates the test files

including test patterns containing IC input patterns and output patterns used by the automatic test

equipment (CL2, L24-29). It would have been obvious to one of ordinary skill in the art at the

time of Applicants' invention to modify the method of **Araki et al.** with the method of **Fusco**

that included the second post-processing tool being another one of an automatic test equipment

(ATE) tester. The artisan would have been motivated because the post processing tool would

analyze the simulation results and generate the test files including test patterns containing IC

input patterns and output patterns used by the automatic test equipment.

8.3   As per Claim 20, **Araki et al.** and **Gruodis et al.** teach the data pattern generator of claim

18. **Araki et al.** teaches that the first post-processing tool is one of a fault simulator (Page 1,

Para 0001. L9-10), and virtual tester (Fig. 5, Item 10; Page 2, Para 0013; Page 2-3, Para 0022).

        Araki et al. does not expressly teach that the first post-processing tool is one of an

automatic test equipment (ATE) tester. **Fusco** teaches that the first post-processing tool is one of

an automatic test equipment (ATE) tester (CL1, L61-65; CL2, L24-39), because the post

processing tool analyzes the simulation results and generates the test files including test patterns

containing IC input patterns and output patterns used by the automatic test equipment (CL2,

L24-29). It would have been obvious to one of ordinary skill in the art at the time of Applicants'

invention to modify the data pattern generator of **Araki et al.** with the data pattern generator of

Fusco that included the first post-processing tool being one of an automatic test equipment

(ATE) tester. The artisan would have been motivated because the post processing tool would

analyze the simulation results and generate the test files including test patterns containing IC

input patterns and output patterns used by the automatic test equipment.

8.4   As per Claim 21, **Araki et al., Gruodis et al.** and **Fusco** each the data pattern generator

of claim 20. **Araki et al.** teaches a fourth plurality of instructions for providing a second

formatted pattern file to a second post-processing tool, the second formatted pattern file based on

the data patterns (Fig. 5, Item 21); and

the second post-processing tool is another one of a fault simulator (Page 1, Para 0001.

L9-10), and virtual tester (Fig. 5, Item 10; Page 2, Para 0013; Page 2-3, Para 0022).

Araki et al. does not expressly teach that the second post-processing tool is another one

of an automatic test equipment (ATE) tester. **Fusco** teaches that the second post-processing tool

is another one of an automatic test equipment (ATE) tester (CL1, L61-65; CL2, L24-39),

because the post processing tool analyzes the simulation results and generates the test files

including test patterns containing IC input patterns and output patterns used by the automatic test

equipment (CL2, L24-29). It would have been obvious to one of ordinary skill in the art at the

time of Applicants' invention to modify the data pattern generator of **Araki et al.** with the data

pattern generator of **Fusco** that included the second post-processing tool being another one of an

automatic test equipment (ATE) tester. The artisan would have been motivated because the post

processing tool would analyze the simulation results and generate the test files including test

patterns containing IC input patterns and output patterns used by the automatic test equipment.

Response to Arguments

9.   Applicant's arguments filed on November 23, 2004 have been fully considered. The

claim rejections under 35 USC 112 Second Paragraph and 35 USC 101 are withdrawn in

response to the Applicants' amendment.   Applicants' argument with respect to claim rejections

under 35 USEC 103 (a) is persuasive.

9.1   As per the applicants' argument that "Reise describes CPU opcodes which are not

generally applicable to use as tester opcodes; CPU opcodes address issues of software

verification, whereas a tester is a piece of hardware in which special functions are invoked with

the use of tester opcodes; Reise does not relate to testers so opcodes described in Reise are not

relevant to Araki", the examiner has used new references, **Gruodis et al.**.

Conclusion

10.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

571-272-3717. The examiner can normally be reached on Monday through Friday from
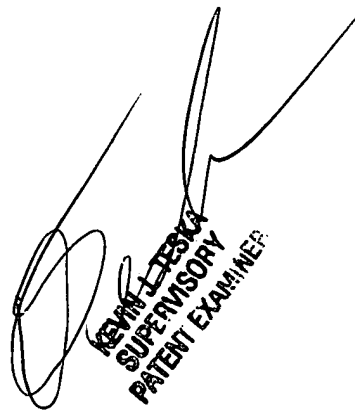
8:00 AM to 5:30 PM.

      If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

      Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-305-

9600.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
February 23, 2005